

TI-SR MPEG 2 Encoder

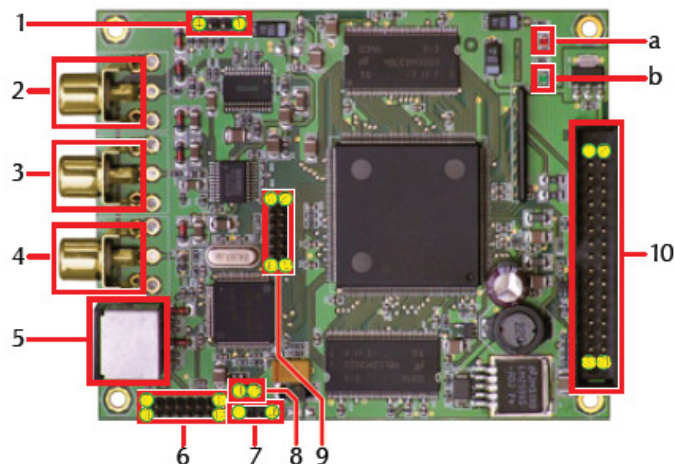
The encoder is based on the Fujitsu MB86391 MPEG-2 system module. This is a dedicated DSP for real-time video compression. Encoder board contains the necessary peripherals, namely, SDRAMs, audio and video codecs as well as the power supply (3.3 and 1.8 V).

The encoder supports formats SIF (352 × 288 pixels), HD1 (352 × 576 pixels) and D1 (720 × 576 pixels) at data rates between 0.5 Mbit / s and 15 Mbit / s. Also included in this data rate is already a 20-bit stereo sound channel. The firmware is loaded by the baseband board at system startup.

It provides a transport stream (SPI) in ISO / IEC 13818 to an 8-bit wide interface with TS clock and Framesync signal.

The video inputs are selectable between composite and Y / C (S-video). Also optional is a parallel input to ITU-656 available.

1 Connector description



board dimensions: 80x100 mm

Connectors	1	4pin Header	ext. I ² C-Bus
	2	RCA plug audio left	0 dB signal level
	3	RCA plug audio right	Signal level adaption only possible after circuit change on the Encoder board!
	4	RCA plug video	Supported standards PAL/NTSC
	5	S-Video	Y/C video input
	6	16pin Header	ext. video and audio input
	7	4pin Header	optional GPIO from video codec
	8	2pin Header	video codec on/off
	9	14pin Header	ITU-656
	10	34pin Header	TS _{out} connection to modulator/multiplexor

LEDs	a	LED red	Voltage 1.8 V ok
	b	LED green	Voltage 3.3 V ok

Developed by SR System GmbH (HW) and Teleinformatica (SW)